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	Subclass
Class	ISSUE CLASSIFICATION



PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.		PATENT DATE
1000	882	Q.A.CTH
SCANNED	2182	2181

APPLICATION NO.	CONT/PRIOR.	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/707585		713	330	2182 2181	Butler

APPLICANTS

Gary Verdun

2185

TITLE

Processor power state transitions using separate logic control

PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)					
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
INTERNATIONAL CLASSIFICATION							
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TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	(Assistant Examiner) _____ (Date)			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent No. _____	(Primary Examiner) _____ (Date)				
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